IN THE CLAIMS:

Please cancel claims 7, 12, and 17, without prejudice.

Please add claims 19 and 20.

1. (Currently amended) A signal phase shifting circuit operative to shift the phase of [an input] a STROBE signal based on a [reference] clock signal comprising:

a [reference] clock signal period dividing circuit having:

a first input that receives the [reference] clock signal,

a second input that receives a feedback control signal,

a phase shift generating circuit operatively responsive to the [reference] clock signal and the feedback control signal;

an output that provides a voltage controlled delay control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal; and

the variable delay circuit including an input that receives the [input] STROBE signal and being operatively responsive to the delay control signal, to provide a phase shifted output signal of the [input] STROBE signal associated with a double data rate communication.

2. (Original) The signal phase shifting circuit of claim 1 wherein the variable delay circuit includes a delay stage and at least one phase shifted output signal drive buffer operatively coupled to the delay stage.

3. (Original) The signal phase shifting circuit of claim 2 wherein the feedback delay matching array includes a plurality of serially coupled buffer stages operatively coupled to compensate for delay variations associated with the at least one phase shifted output signal drive buffer.

4. (Currently amended) The signal phase shifting circuit of claim 1 wherein the variable delay circuit includes a delay stage and at least one [mulitplexer] multiplexer operatively coupled to vary a delay setting of the variable delay stage, and at least one

phase shifted output signal drive buffer operatively coupled to an output of the at least one [mulitplexer] multiplexer.

5. (Currently amended) The signal phase shifting circuit of claim 4 wherein the feedback delay matching array includes a plurality of serially coupled [mulitplexer] multiplexer and buffer stages operatively coupled to compensate for delay variations associated with the at least one [mulitplexer] multiplexer and the at least one phase shifted output signal drive buffer in the variable delay circuit.

6. (Currently amended) The signal phase shifting circuit of claim 1 including a data latch having a first input operatively coupled to receive data, and a second input operatively coupled to receive the phase shifted output signal of the STROBE signal.

7. (Canceled).

8. (Currently amended) The signal phase shifting circuit of claim 1 wherein the phase shift generating circuit includes a plurality of serially coupled buffers that form a controlled delay stage and wherein the feedback delay matching array includes a plurality of serially coupled [mulitplexer] multiplexer and buffer stages operatively coupled to the plurality of serially coupled buffers.

9. (Currently amended) A signal phase shifting circuit operative to shift the phase of a [strobe] STROBE signal based on a [reference] clock signal comprising:

a reference signal period dividing circuit having:

a first input that receives the [reference] clock signal,

a second input that receives a feedback control signal,

a phase shift generating circuit that includes a delay lock loop circuit operatively responsive to the reference signal and the feedback control signal wherein the delay lock loop circuit includes:

a phase/frequency detection circuit that compares the reference signal and the feedback control signal,

a charge pump circuit operatively coupled to the phase/frequency detection circuit, and

a loop filter operatively responsive to an output from the charge pump circuit, that provides a delay control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal; and

the variable delay circuit including an input that receives the [input] STROBE signal and being operatively responsive to the delay control signal, to provide a phase shifted output signal of the STROBE signal.

10. (Currently amended) The signal phase shifting circuit of claim 9 wherein the variable delay circuit includes a delay stage and at least one [mulitplexer] multiplexer operatively coupled to vary a delay setting of the variable delay stage, and at least one phase shifted output signal drive buffer operatively coupled to an output of the at least one [mulitplexer] multiplexer.

11. (Currently amended) The signal phase shifting circuit of claim 10 wherein the feedback delay matching array includes a plurality of serially coupled [mulitplexer] multiplexer and buffer stages operatively coupled to compensate for delay variations associated with the at least one [mulitplexer] multiplexer and the at least one phase shifted output signal drive buffer in the variable delay circuit.

12. (Canceled).

13. (Currently amended) The signal phase shifting circuit of claim 9 wherein the phase shift generating circuit includes a plurality of serially coupled buffers that form a controlled delay stage and wherein the feedback delay matching array includes a plurality of serially coupled [mulitplexer] multiplexer and buffer stages operatively coupled to the plurality of serially coupled buffers.

14. (Currently amended) A data receiving circuit having a signal phase shifting circuit operative to shift the phase of a [strobe] STROBE signal based on a [reference] clock signal comprising:

a reference signal period dividing circuit having:

a first input that receives the [reference] clock signal,

a second input that receives a feedback control signal,

a phase shift generating circuit that includes a delay lock loop circuit operatively responsive to the reference signal and the feedback control signal wherein the delay lock loop circuit includes:

a phase/frequency detection circuit that compares the reference signal and the feedback control signal,

a charge pump circuit operatively coupled to the phase/frequency detection circuit, and

a loop filter operatively responsive to an output from the charge pump circuit, that provides a control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal;

the variable delay circuit being operatively responsive to the control signal that provides a phase shifted output signal, and including an input that receives the [input] STROBE signal; and

a data latch having a first input operatively coupled to receive data, and a second input operatively coupled to receive the phase shifted output signal.

15. (Currently amended) The signal phase shifting circuit of claim 14 wherein the variable delay circuit includes a delay stage and at least one [mulitplexer] multiplexer operatively coupled to vary a delay setting of the variable delay stage, and at least one

phase shifted output signal drive buffer operatively coupled to an output of the at least one [mulitplexer] multiplexer.

16. (Currently amended) The signal phase shifting circuit of claim 15 wherein the feedback delay matching array includes a plurality of serially coupled [mulitplexer] multiplexer and buffer stages operatively coupled to compensate for delay variations associated with the at least one [mulitplexer] multiplexer and the at least one phase shifted output signal drive buffer in the variable delay circuit.

17. (Canceled).

18. (Currently amended) The signal phase shifting circuit of claim 14 wherein the phase shift generating circuit includes a plurality of serially coupled buffers that form a controlled delay stage and wherein the feedback delay matching array includes a plurality of serially coupled [mulitplexer] multiplexer and buffer stages operatively coupled to the plurality of serially coupled buffers.

19. 19. (New) depend on 1 A signal phase shifting circuit operative to shift the phase of [an input] a STROBE signal based on a [reference] clock signal comprising:

a [reference] clock signal period dividing circuit having:

a first input that receives the [reference] clock signal,

a second input that receives a feedback control signal,

a phase shift generating circuit operatively responsive to the [reference] clock signal and the feedback control signal;

an output that provides a voltage controlled delay control signal for a variable delay circuit, and

a feedback delay matching array operatively coupled to an output of the phase shift generating circuit, that produces the feedback control signal; and

the variable delay circuit including an input that receives the [input] STROBE signal and being operatively responsive to the delay control signal, to provide a phase shifted output signal of the [input] STROBE signal associated with a double data rate communication.

19. (New) The signal phase shifting circuit of claim 1 wherein the feedback delay matching array includes a number of serially coupled multiplexers and buffers such that the number of serially coupled multiplexers and buffers and a predetermined fraction of a clock period are reciprocals of one another.

20. (New) The signal phase shifting circuit of claim 9 wherein the feedback delay matching array includes a number of serially coupled multiplexers and buffers such that the number of serially coupled multiplexers and buffers and a predetermined fraction of a clock period are reciprocals of one another.